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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,602	11/14/2001	Wingyu Leung	MST-012	4719

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EXAMINER	
TU, CHRISTINE TRINH LE	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,602	LEUNG ET AL.	
	Examiner	Art Unit	
	Christine T. Tu	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5 and 7* is/are allowed.

6)☒ Claim(s) *6,8-10,13-15 and 17-20* is/are rejected.

7)☒ Claim(s) *11-12, 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/14/01; 2/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

5.00

DETAILED ACTION

1. Claim 1 are objected to because of the following informalities:

Claim 1:

At lines 19-20, the term "first storage circuit" should be replaced with –first register--.

Appropriate correction is required.

2. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 (depend on claim 2):

Claim 6 cannot depend on a cancelled claimed (claim 2).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzales et al (6,101,614 and Gonzales hereinafter) in view of White (4,345,328).

Claim 8:

Gonzales discloses the invention substantially as claimed. Gonzales teaches (figures 1-3) a computer system comprising a memory controller (MC) for handling memory access requests and memory interface components (MICs) for interfacing the MC to a memory array. The MC is divided into separate components naming as a DRAM controller (DC) and a data path (DP). When writing data, data is first popped off to a write data buffer (in the DP) and then input to the ECC code word generation unit where 8 parity bits are calculated and appended to the DWORD to form a 72 bit code where that is subsequently written to the memory array (figures 1, 2 and 3, column 4 lines 14-23 and 54-62, column 6 lines 60-67).

Gonzales does not explicitly teach that the write buffer also receives and stores a write address value. However, Gonzales teaches that the DRAM controller (DC) is consisted of a queue management unit (QMUC) for buffering addresses received from a bus engine (BEC) into a memory interface (MMIC) (column 5 lines 21-25, column 5 lines 38-44). It would have been obvious to one skilled in the art at the time the invention was made to combine both Gonzales' write data buffer and Gonzales' QMUC together for storing both the data and the corresponding addresses. The artisan would have been motivated to do so because Gonzales suggests not only the MC can divided

into separate components (DC and DP), but also can be implemented as a single package (column 5 lines 2-8).

Gonzales does not explicitly teach the feature of providing the ECC value as long as the first write data value is stored in the first register. White, however, teaches the feature of providing check bits (of a data word) by an ECC generator (203) via a cable (103) while the data-in register (100) provides the data word via another cable (103) (figure 2, column 2 lines 63-64). It would have been obvious to one skilled in the art at the time the invention was made to use two cables as taught by White for providing check bits and data words separately in Gonzales's MC. One having ordinary skill in the art would be motivated to do so because together or separately providing the data and the corresponding check bits would have been a design choice and such a choice would not affect the content of the data as a whole.

Claim 9:

Gonzales teaches that each set of data buffer comprises four buffers, any number of read and write data buffers may be used in a pipelined system (column 6 lines 11-15).

Gonzales also teaches that a set of write data buffers (in the QMUD) temporarily buffers write data received from the system bus before it is written to the memory. Such set of buffers may be used in a pipelined system such that a total of eight different memory accesses may be in process at one time (column 6 lines 4-16).

Claim 10:

Gonzales does not explicitly teach the enabling tri-state buffers during the write access. Gonzales, however, teaches a set of four data buffers for buffering write data received from the system bus before it is written to the memory wherein the buffers are used in a pipelined system (column 6 lines 4-16). It would have been obvious to one skilled in the art at the time the invention was made to use the tri-state buffers. The artisan would have been motivated to do so because (1) tri-state buffers are well-known in the art, and (2) Gonzales's write data buffers do not exclude from the inclusion of tri-state buffers.

5. Claims 13-15 and 17-20 are again rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzales et al (6,101,614 and Gonzales hereinafter).

Claims 13-15 and 17-20:

The rationale for rejecting these claims is again the same as it was set forth in paragraph 3 of the previous office action which was mailed on August 24, 2004.

Response to Arguments

6. Applicant's arguments with respect to claims 10-12 have been considered but are moot in view of the new ground(s) of rejection.

For claims 1-7, applicant argues that Gonzales fails to disclose the "means for outputting" as being recited in the amended claims. Examiner agrees with applicant's remark. Gonzales does fail to teach the means for outputting the write data value and the ECC value during a read access if a read address value associated with the read access matches the first write address value stored in the first storage circuit.

For claim 8, applicant also argues that Gonzales fails to disclose that the ECC generator being configured to provide the first ECC value as long as the first write data value is stored in the first register. However, such limitation is taught by the combination of Gonzales and White (see ¶4 above).

For claims 13-20, applicant further alleges that the reference of Gonzales fails to teach limitation of "a write-back buffer configured to store the corrected first data/ECC value in response to the asserted error indicator signal". Applicant should aware that throughout claims 13 and 17-20, slashes "/" are being used in many terms. Such slashes "/" can be interpreted as "or" (which is an alternative term) by Examiner. Because of the use of a slash "/" in the claimed language "a write-back buffer configured to store the corrected first data / ECC value...", the examiner can interpret the limitation

as "a write-back buffer stores the corrected first data **or** ECC value...". Therefore, any reference either showing the storing of the corrected data, or showing the storing of ECC value can be used for art rejection. Such a limitation of storing the corrected data in a write-back buffer is now suggested by Gonzales (column 7 lines 46-50, and column 8 lines 23-33). Gonzales suggested the read data buffers in the QMUD such one of the read data buffers stores the corrected data and then sends the corrected data back to the memory (as being rejected in ¶3 of the previous office action [mailed 8/24/2004]).

Applicant is requested to review the use of all slashes "/" (which means alternative) in claims 13 and 17-20 to make sure whether or not that is the way applicant would like the claims to be recited.

7. Claims 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 1-5 and 7 are allowable over the prior arts.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christine T. Tu
Primary Examiner
Art Unit 2133

May 25, 2005